

Jan. 31, 1967

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3,302,039

GATEABLE BRIDGE NETWORK HAVING POWER GAIN

Filed Feb. 17, 1964

3 Sheets-Sheet 1

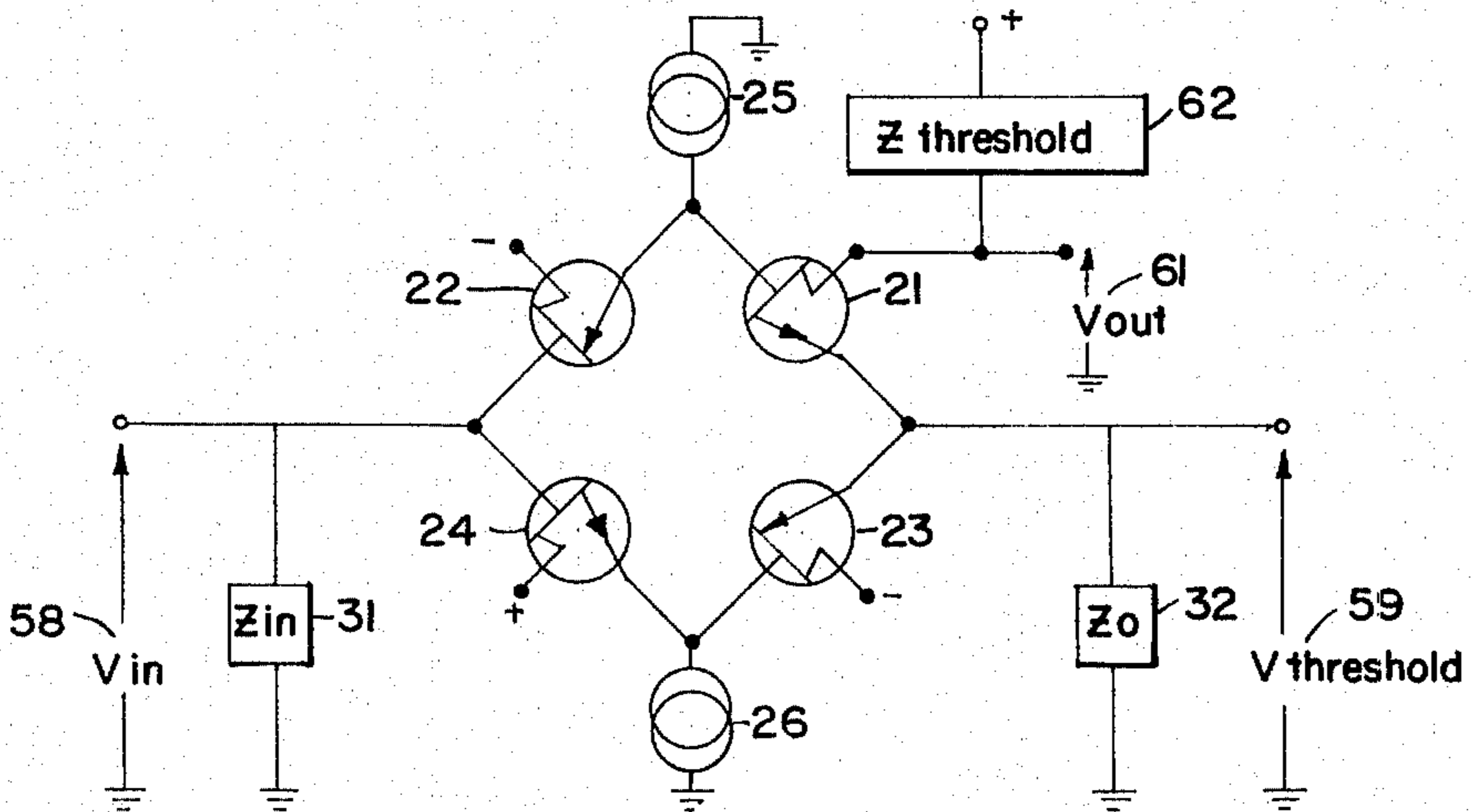
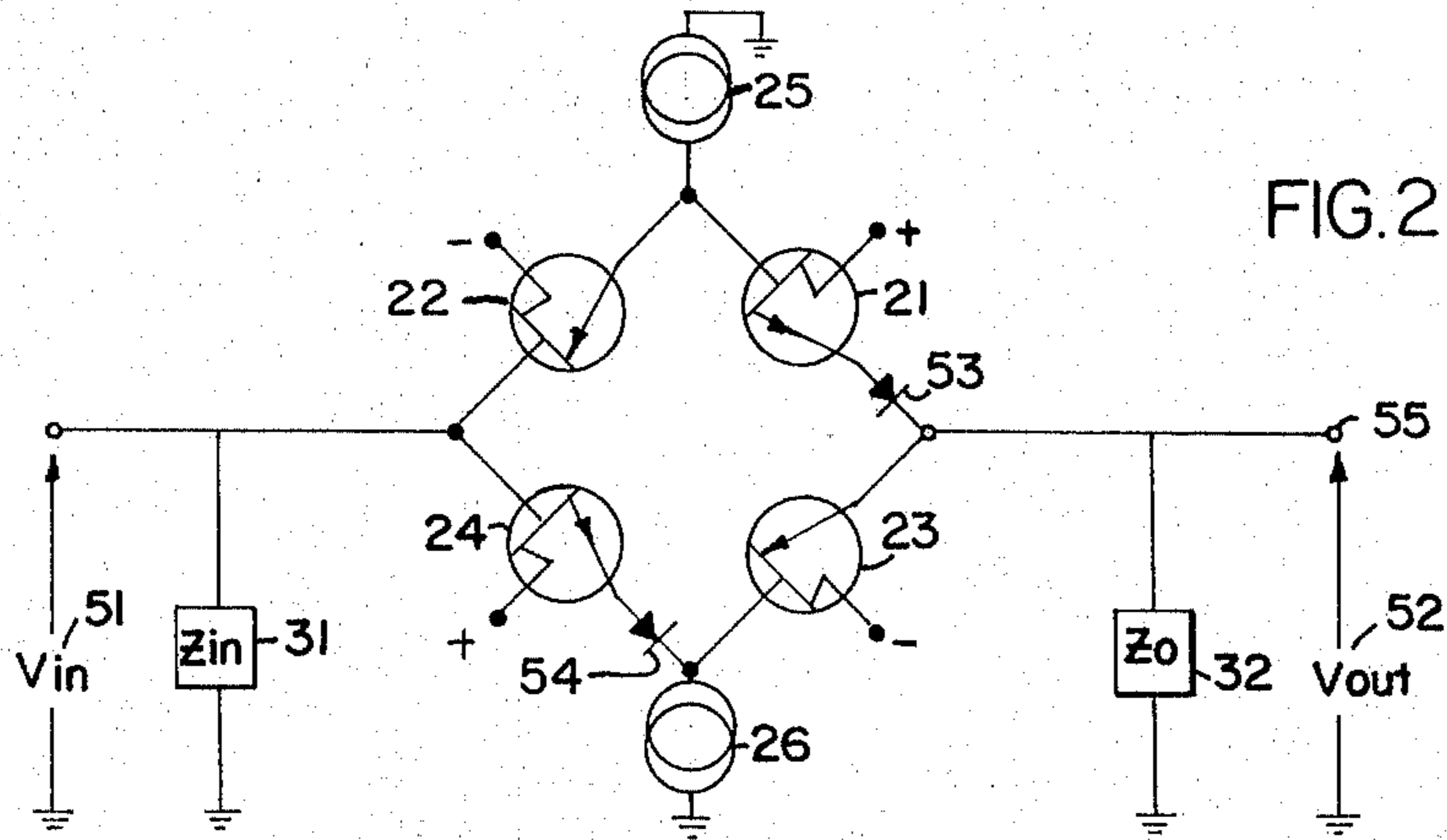
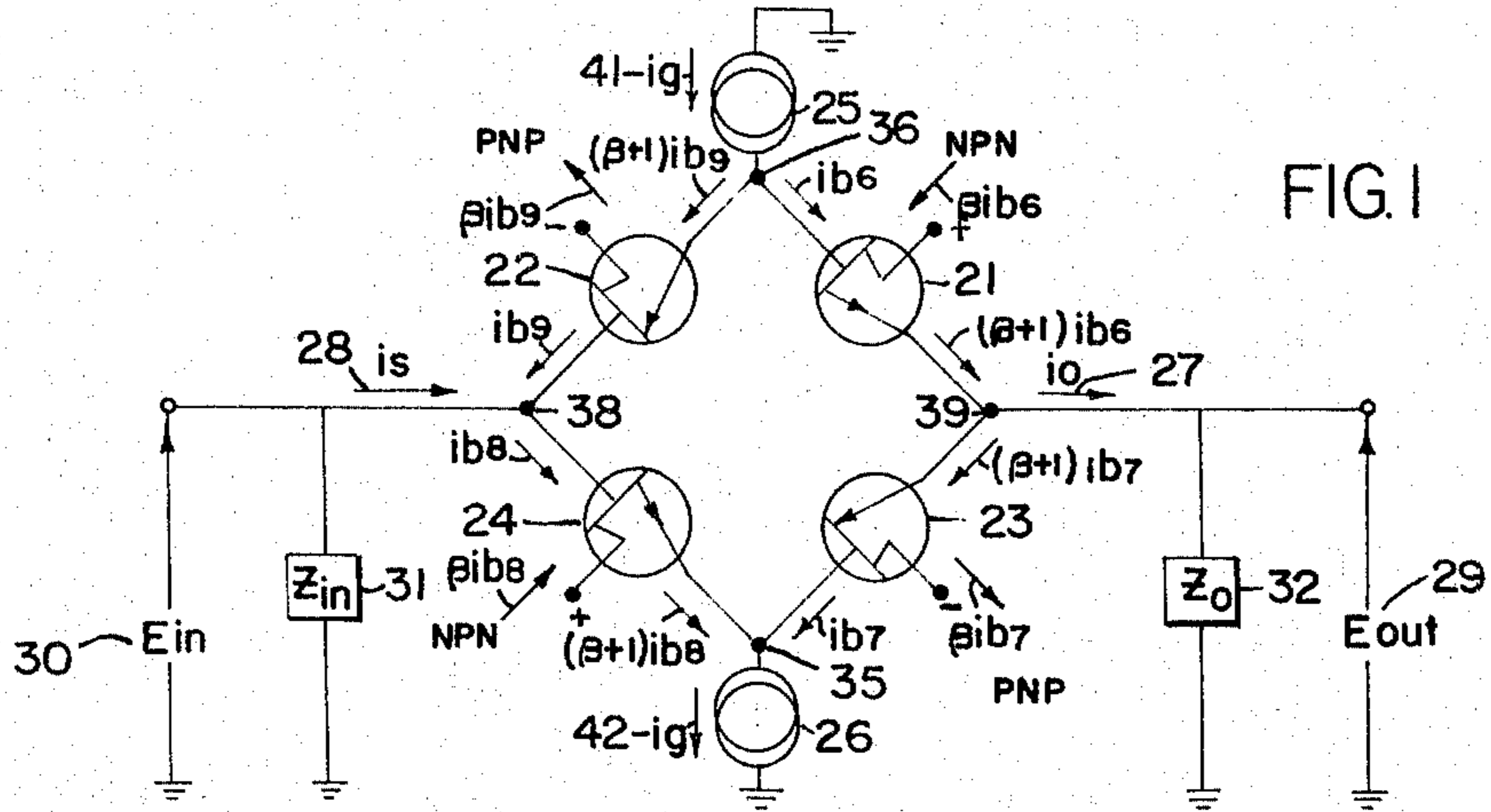


FIG. 3

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3 Sheets-Sheet 2

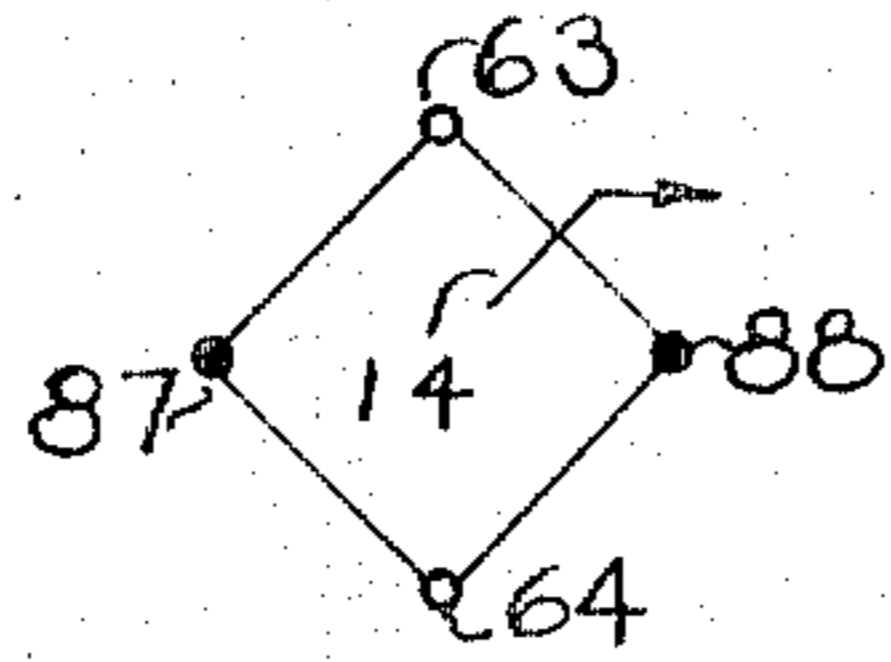
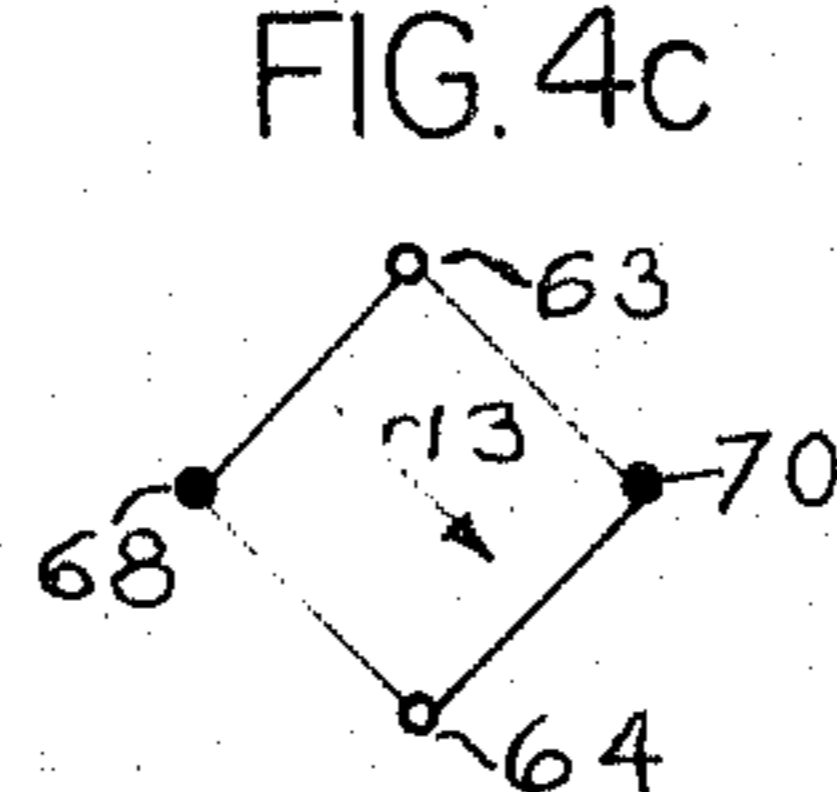
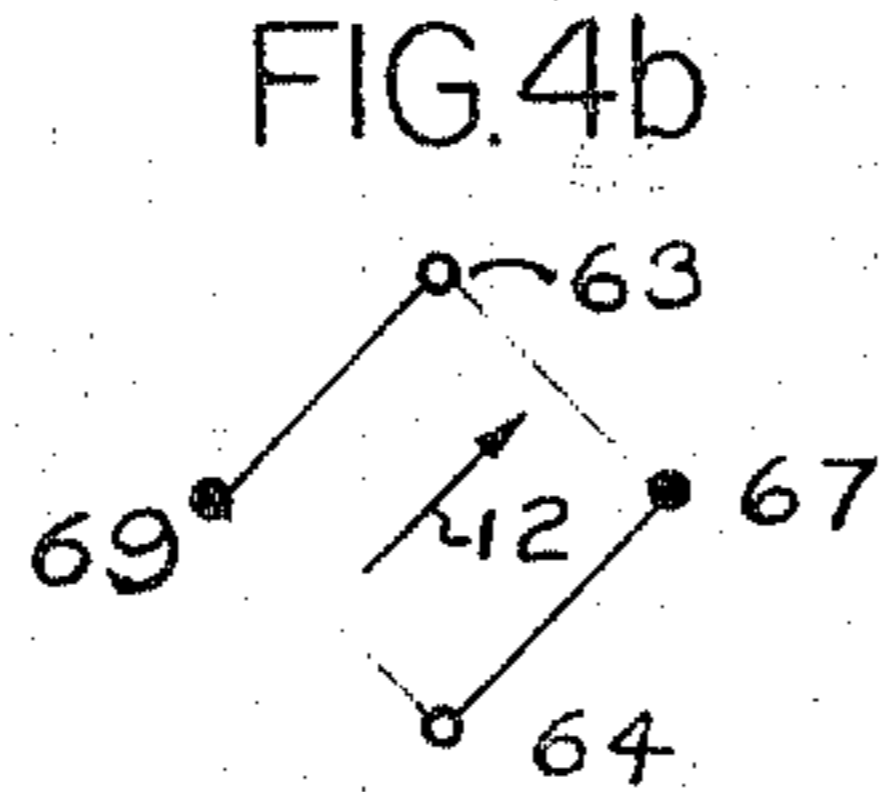
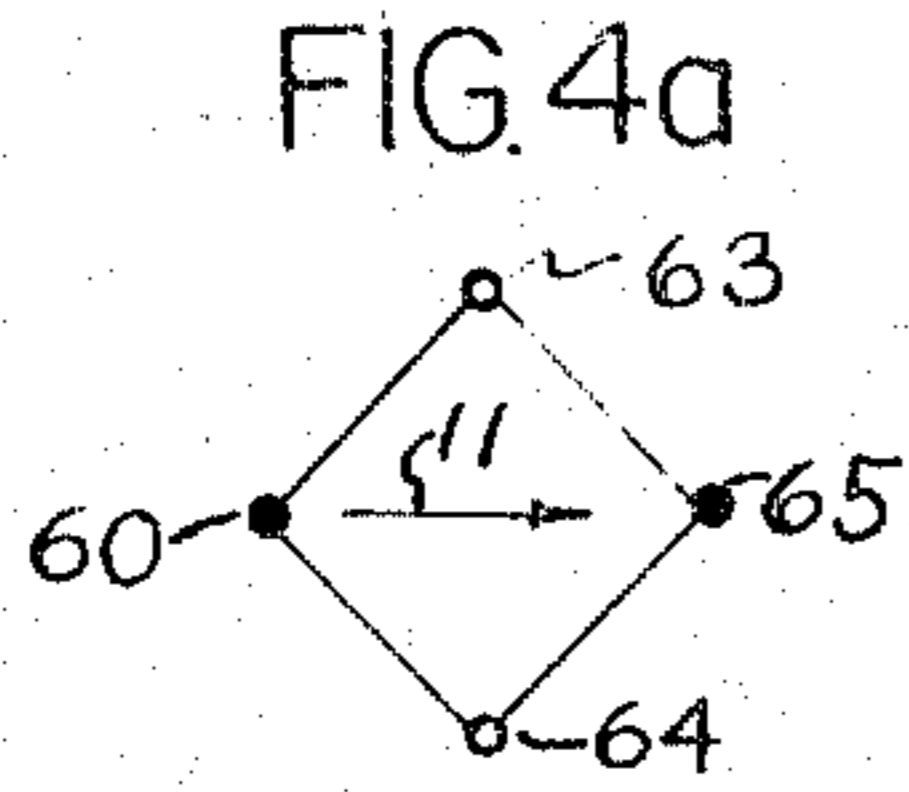


FIG. 4d

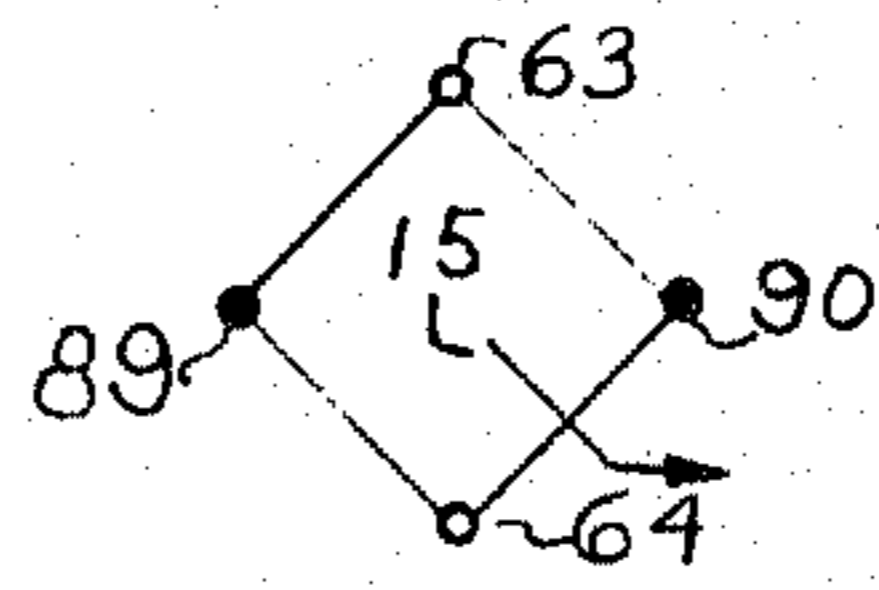


FIG. 4e

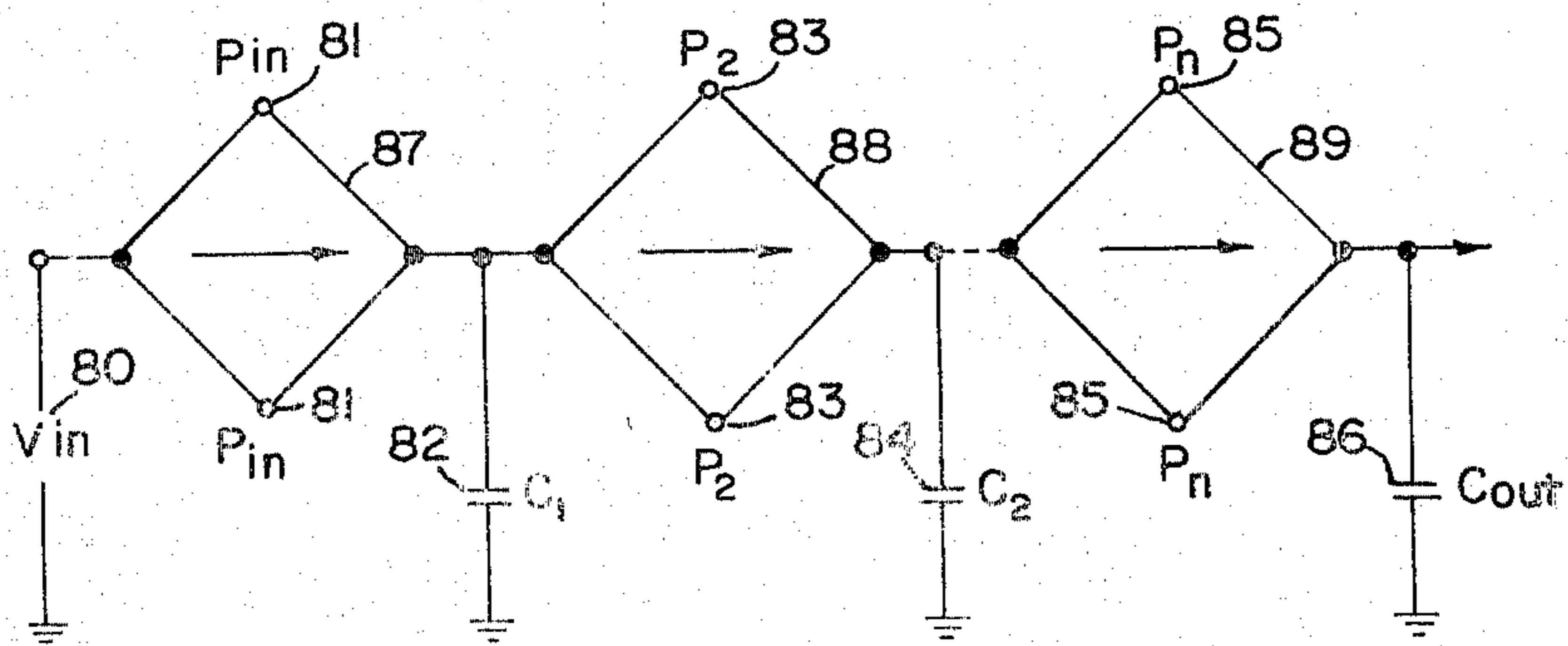
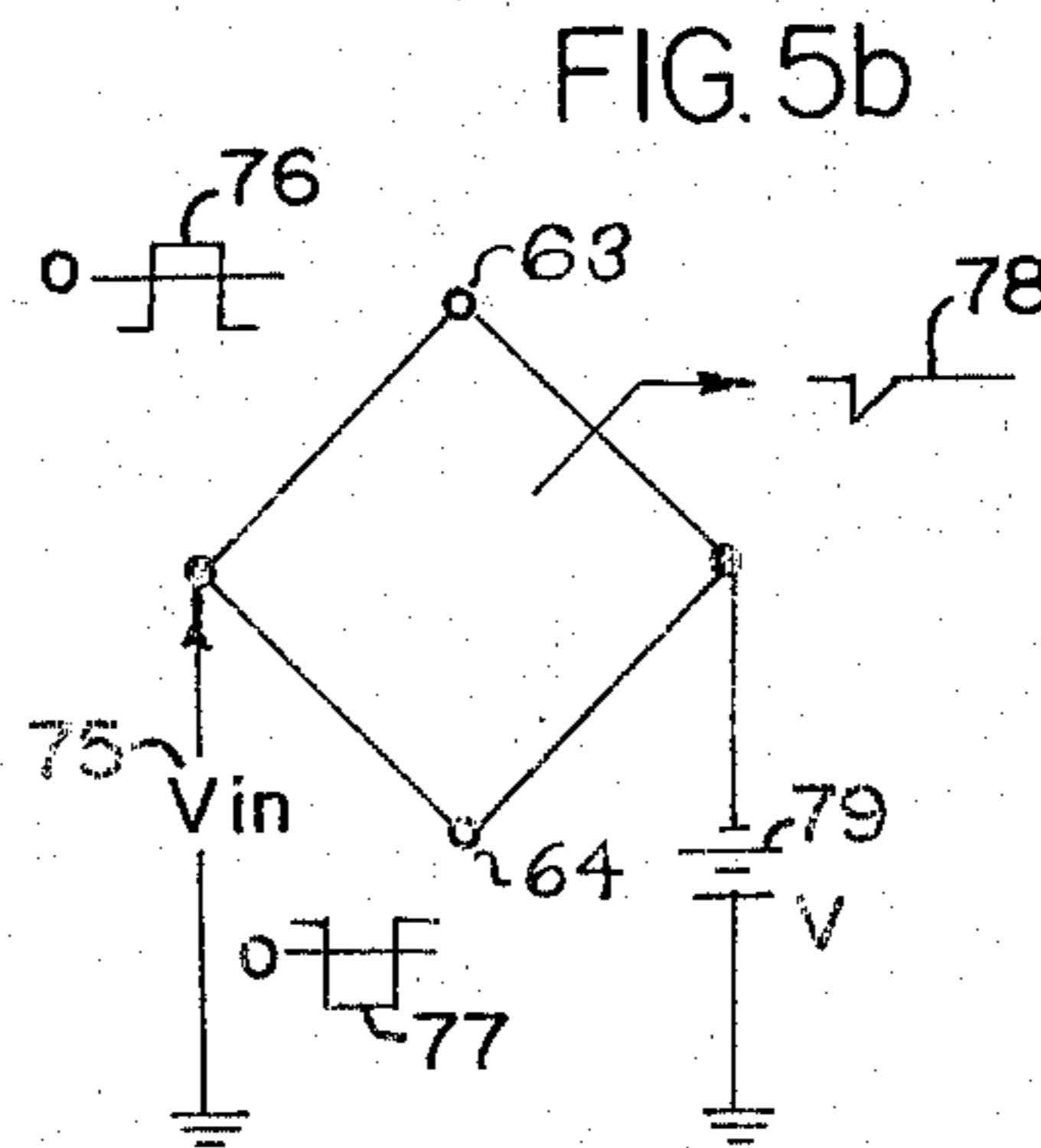
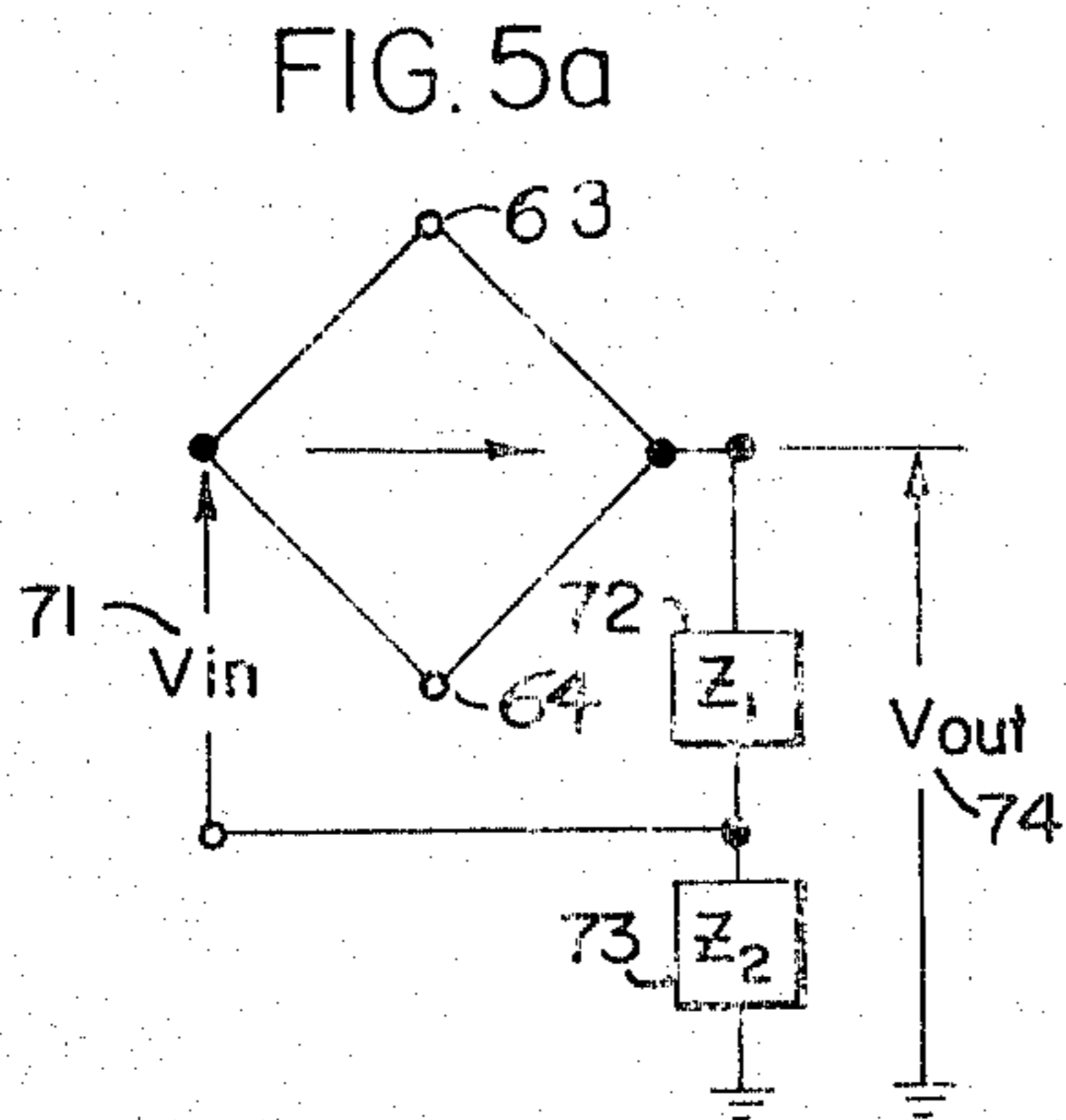


FIG. 5c

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GATEABLE BRIDGE NETWORK HAVING POWER GAIN

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3 Sheets-Sheet 3

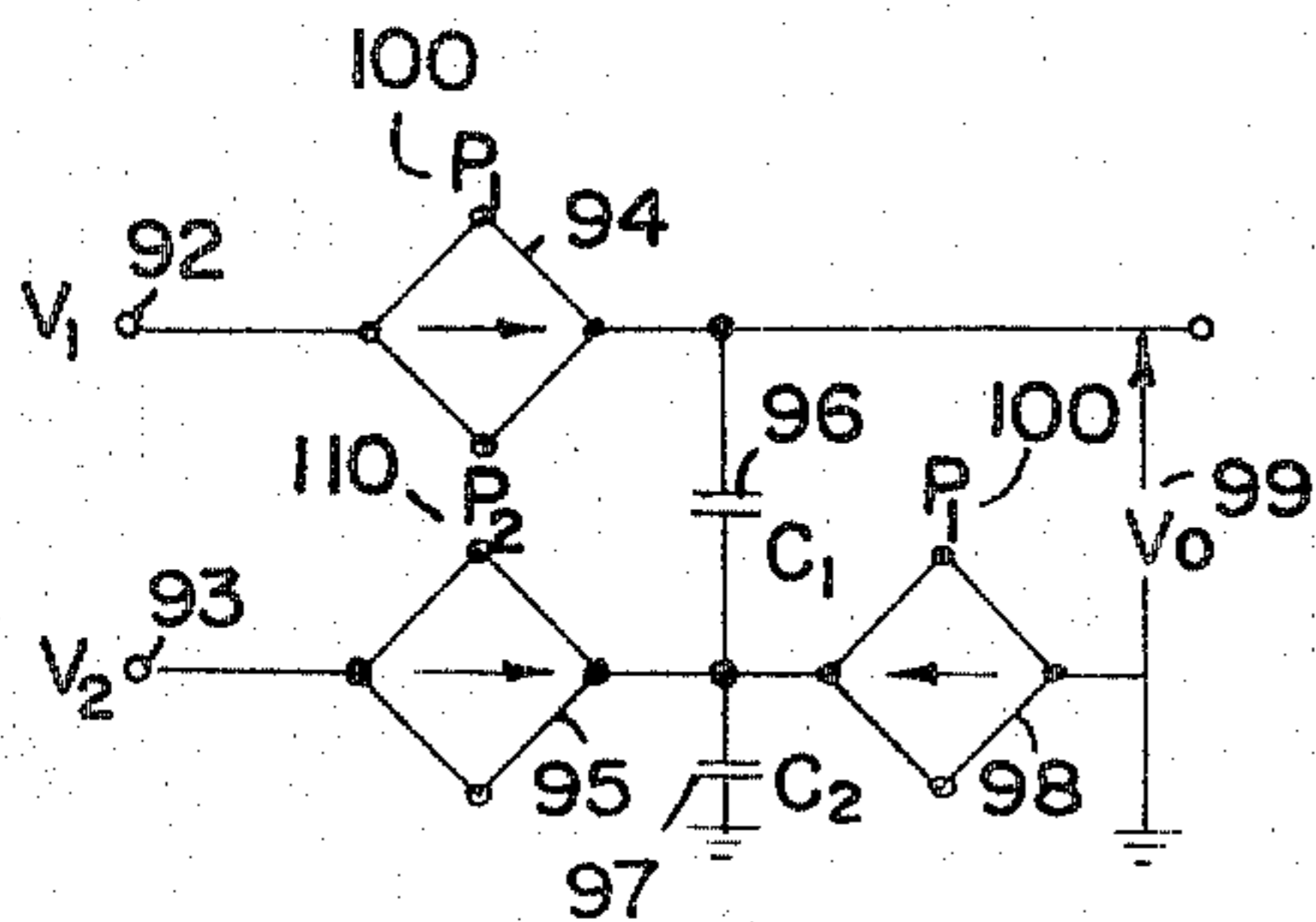


FIG. 5d

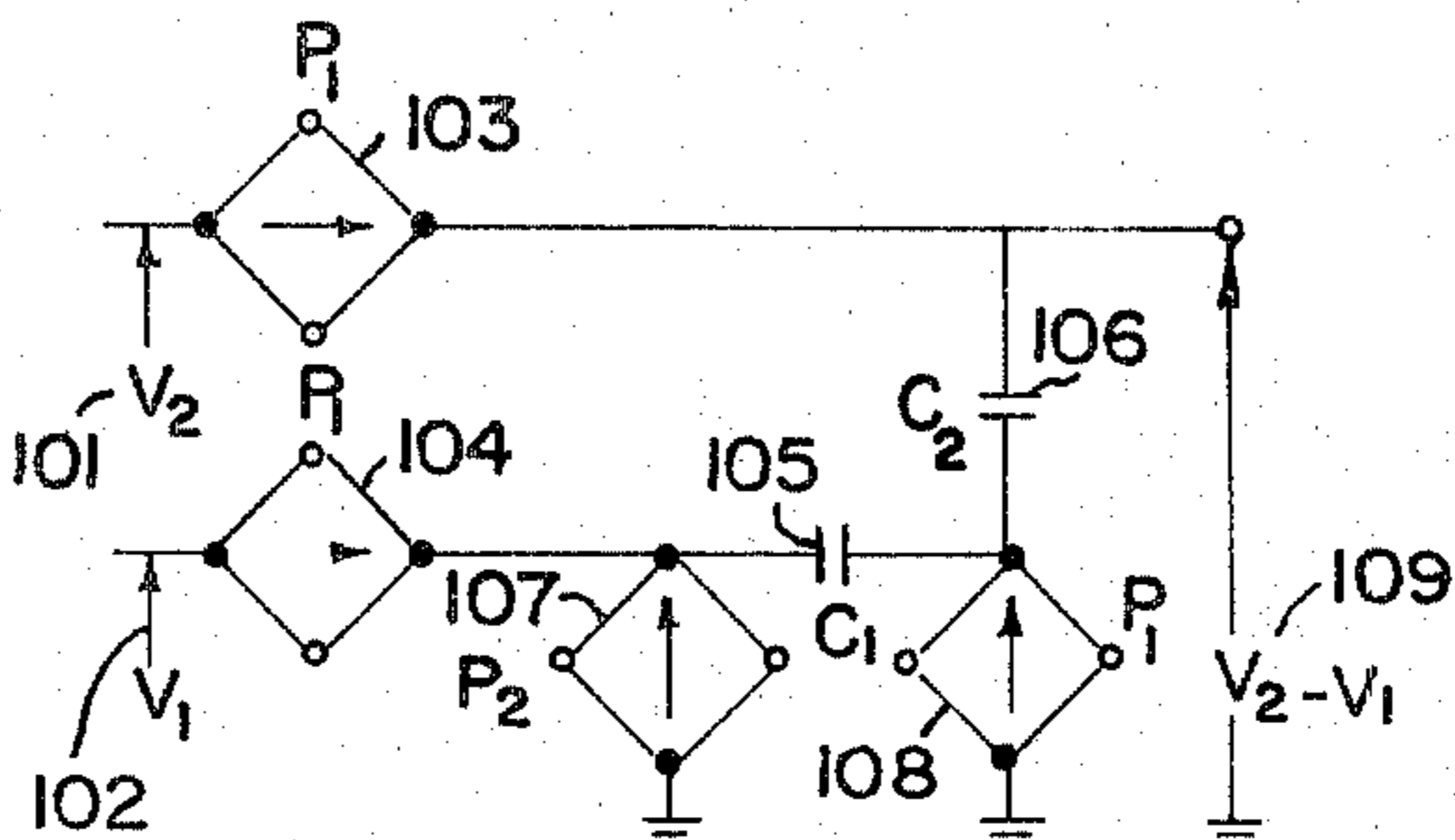


FIG. 5e

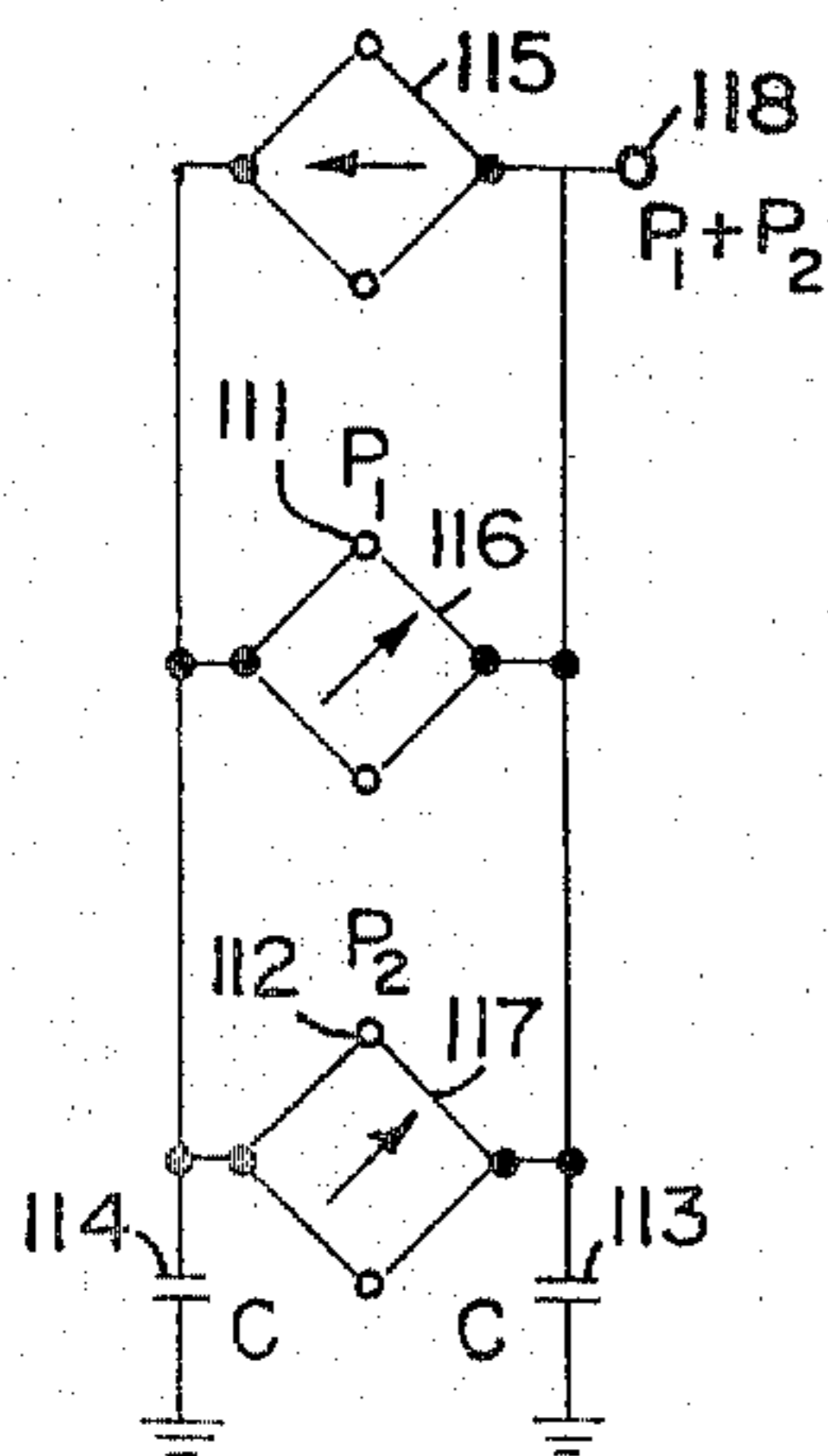


FIG. 5f

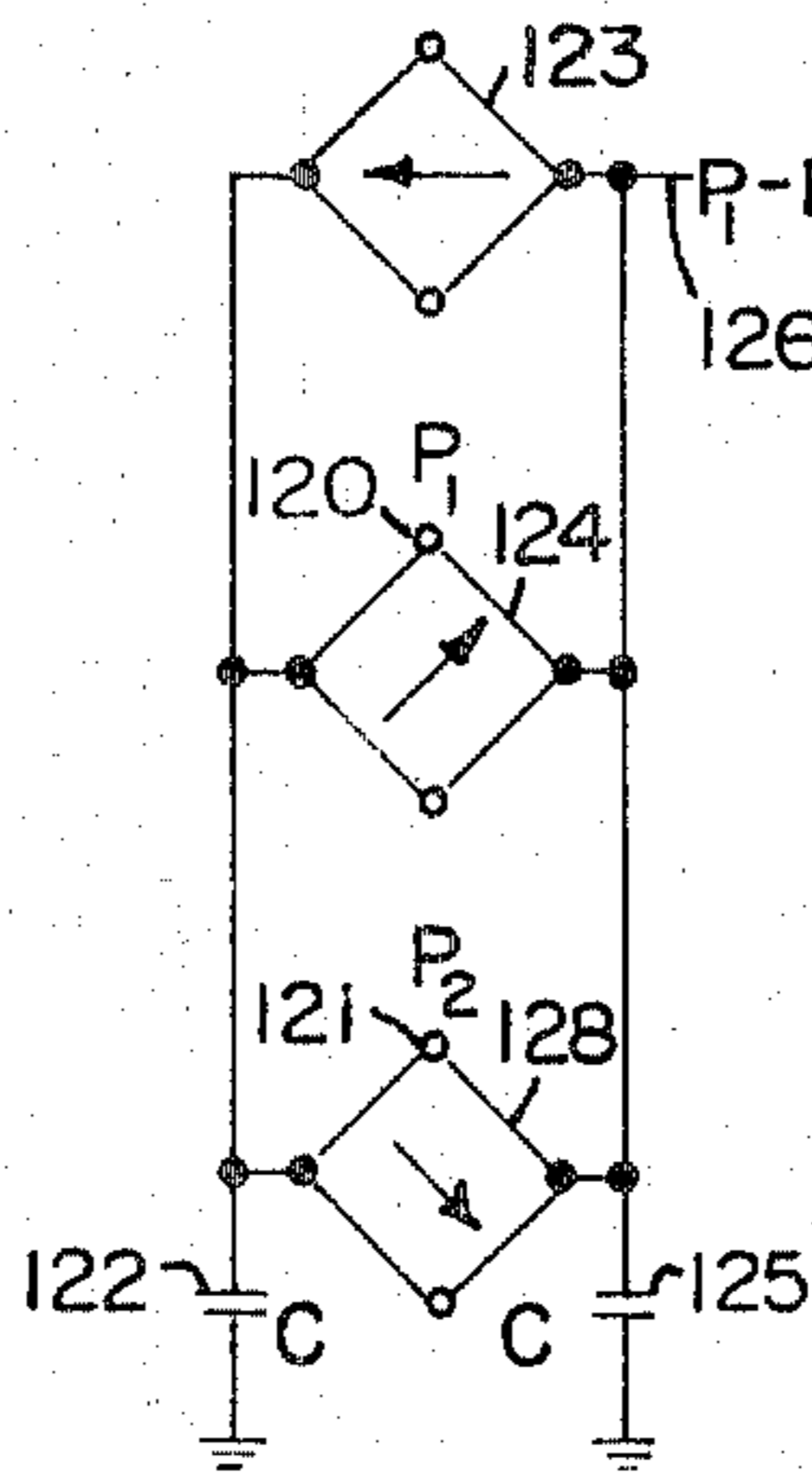


FIG. 5g

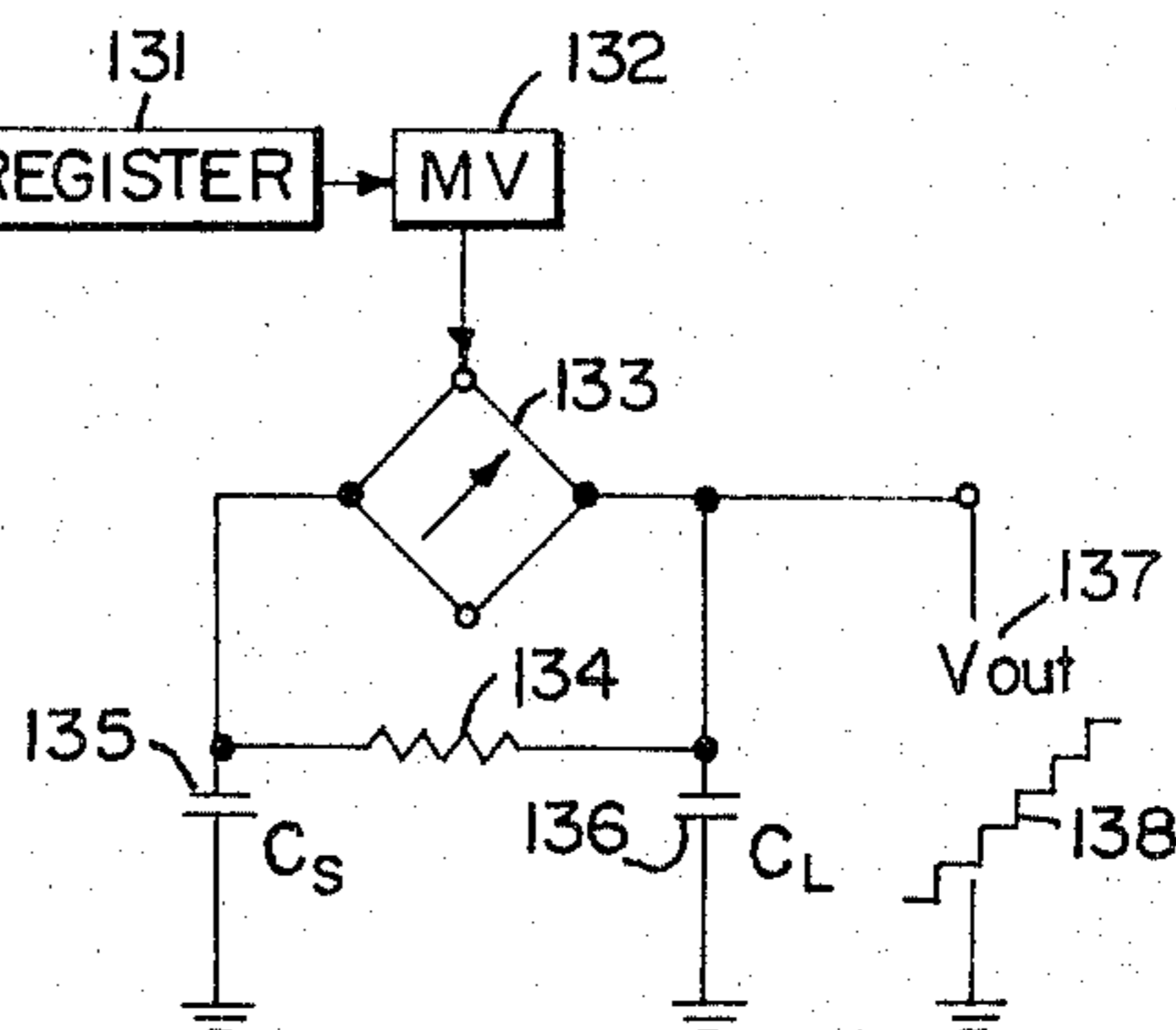


FIG. 5h

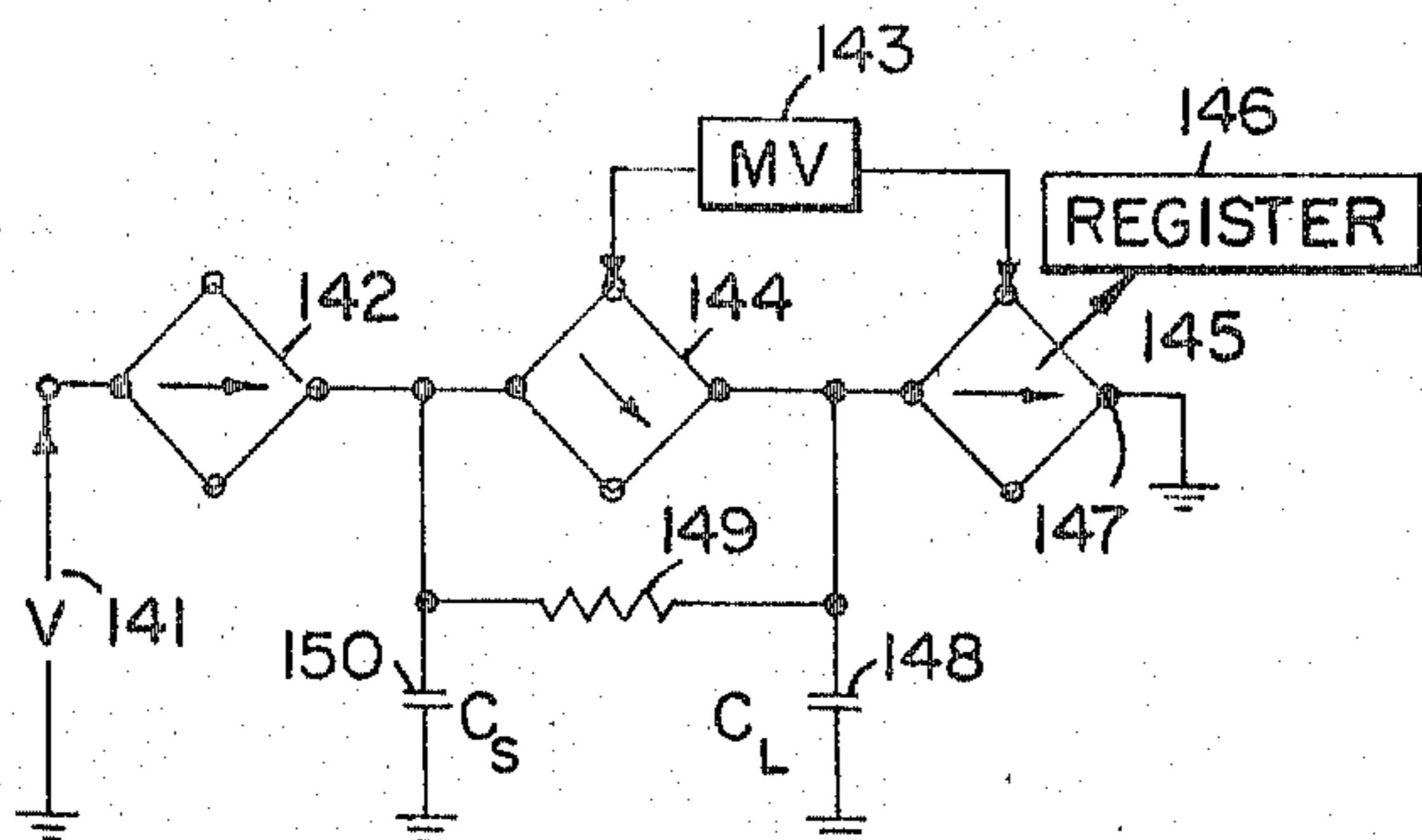


FIG. 5j

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## GATEABLE BRIDGE NETWORK HAVING POWER GAIN

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5 Claims. (Cl. 307-88.5)

The present invention relates to bridge networks, and more particularly to bridge networks employing gain-producing elements to provide systems which perform both analog and digital functions.

Analog techniques, on the one hand, are superior to digital techniques in that such systems are much more easily synthesized. The foregoing is particularly true in real time processing. Digital techniques, on the other hand, offer the advantages of reliability, simplicity of circuit design, and provide a building block approach to system design.

The present invention provides a circuit having some of the advantages of both digital and analog techniques, such as the use of continuously variable threshold levels in analog operation. This mode of operation is often desirable in signal detection in order to avoid the necessity for quantizing the signal and to avoid the complexity inherent in the analog to digital conversion process.

Networks according to the invention are also well adapted to use with the discrete threshold levels of digital circuitry and thus permit the building block approach to system synthesis. The provision of both analog and digital functions permits my networks to perform digital to analog or analog to digital conversions with a minimum of system complexity. Input-output isolation and adaptability to clock pulse control are provided by my invention with both the analog and digital functions. Therefore, advantages of the digital building block system approach can be utilized in systems which function in an analog manner. The reduction in system complexity permits power consumption to be held to a minimum so that systems incorporating my invention are well adapted for use in space or other remote locations.

In general, my invention is characterized by a novel gain-producing bridge network capable of effective operation in floating or above-ground condition while providing substantial power gain in accurately transferring the input signal to the output. This makes possible simple but accurate systems operating in analog or digital modes depending on the particular function desired. By way of example, circuits utilizing the present invention may provide a highly effective isolation amplifier; a function generator (D.-C. or A.-C. amplifier with or without feedback or a ladder); a linear slope generator; delay and storage circuits; digital-to-analog converters; analog-to-digital converters; and simple but effective adder, subtractor, multiplier, and divider circuits. Furthermore, systems using the present invention permit a marked reduction in complexity and power consumption, while providing excellent stability.

In accordance with the foregoing, my invention has as an object the provision of a novel gain-producing isolation and control circuit which makes possible the provision of a wide variety of systems having analog and digital functions.

Another object is to provide reliable high-speed circuit modules.

Another object is the provision of easily fabricated digital and analog systems which have low power consumption.

A further object is to provide interchangeable circuit modules performing analog or digital functions.

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Still another object is the provision of circuit modules which permit a building-block approach to the design of analog systems.

A still further object is the provision of detection and transfer circuits with adjustable threshold levels.

Still another object is the provision of reliable transfer circuits which shift the input voltage in predetermined voltage increments.

Other objects and features will appear from the following description, taken in connection with the accompanying drawings in which:

FIGURE 1 shows the basic circuit configuration.

FIGURE 2 shows the basic circuit with provision for the insertion of an offset voltage in the output voltage.

FIGURE 3 shows the basic circuit with provisions for the establishment of a threshold voltage.

FIGURE 4 shows symbolic representations of the various sub-system configurations wherein:

FIGURE 4A is the basic straight-through bridge.

FIGURE 4B is the same circuit with positive offset.

FIGURE 4C shows a circuit similar to 4B but with negative offset.

FIGURE 4D is a circuit showing the establishment of a positive threshold.

FIGURE 4E is a circuit showing the establishment of a negative threshold.

FIGURE 5 illustrates numerous applications of the various sub-systems depicted in FIGURE 4 where representative functions are performed as follows:

FIGURE 5A shows a basic voltage amplifier.

FIGURE 5B shows a threshold detection circuit.

FIGURE 5C is a storage circuit.

FIGURE 5D represents an analog addition circuit.

FIGURE 5E is an analog subtraction circuit.

FIGURE 5F is a digital addition circuit.

FIGURE 5G is a digital subtraction circuit.

FIGURE 5H is a digital-to-analog converter.

FIGURE 5J is an analog-to-digital converter.

The basic circuit configuration, illustrated in FIG. 1, is characterized by a four terminal bridge or diamond configuration wherein the arms include transistors or other gain-producing elements. Moreover, a control current is applied to terminals other than the input and output terminals. This control current may be pulsed or continuous and controls the transfer of the signal from input to output and the control current is applied in such a manner that the bridge effectively "floats" above ground. The bridge therefore provides controlled sampling with power gain. The use of transistors results in a mode of operation different from that of conventional bridge circuits.

The basic bridge configuration will first be described. Four nodes 35, 36, 38, 39 to which four transistors are interconnected form the legs of the bridge. The bases of transistors 22 and 24 are connected to input node 38. The emitters of transistors 21 and 23 are connected to output node 39. The base of transistor 21 and the emitter of transistor 22 are connected to node 36, and the base of transistor 23 and emitter of transistor 24 are connected to node 35.

Current  $i_{g28}$  is the current that flows from the input source into the bridge circuit at node 38 and correspondingly,  $i_{o27}$  is the output current that flows from the bridge circuit at node 39. Current  $i_{g41}$  generated at current source 25 flows into the bridge at node 36. Current  $i_{g42}$  generated at current source 26 flows out of the bridge circuit at node 35.

Currents  $i_b6, 7, 8$  and  $9$  are those which flow within the bridge and are related to signal source current  $i_{g28}$ , the load current  $i_{o27}$ , and both  $i_{g41}$  and  $i_{g42}$  which are generated by the current sources 25 and 26.  $i_b6, 7, 8$  and  $9$

are collector currents that enter or leave the circuit, depending upon the indicated polarity at the collectors of the transistors.

Assume an input signal  $E_{in30}$  applied by way of input impedance  $Z_{in31}$  at node 38 and that current generators 25 and 26 are off. Then  $i_b$  in the leg containing transistor 22 and the leg containing transistor 24 will be zero, for the current sources 25 and 26 block the path to ground in these respective branches of the circuit. Further tracing of the circuit shows that the current is blocked by means of transistors 22 and 23 in the paths to ground by way of load impedance  $Z_{o32}$ .

When current sources 25 and 26 are turned on, currents  $i_{g41}$  and  $i_{g42}$  will flow into and out of the circuit respectively. As will be explained more fully,  $E_{in30}$  is effectively transferred to the output side and appears as  $E_{out29}$ .  $E_{in30}$  and  $E_{out29}$  differ by some small quantity due to the uncertainty of the components which for the most part can be ignored. This difference may be negative or positive and, when several units are coupled together, differences tend to cancel.

To continue in this analysis, assume that  $E_{in30}$  is continuously applied to the circuit and that current sources 25 and 26 are switched on for a short period of time.  $E_{in30}$  appears across the bridge arms including transistors 22 and 21 and bridge arms including transistors 24 and 23 from node 38 to ground through node 39 and load impedance  $Z_{o32}$ . Assume the polarity of  $E_{in30}$  holds transistor 22 off and transistor 24 on. Consequently,  $i_{s28}$  is related directly to  $i_{g42}$  by way of the amplification factor of transistor 24. It will be shown that

$$\frac{i_{s28}}{\beta} \cong i_{g42}$$

where  $\beta$  is the amplification factor of the transistor.

During transition (i.e. while  $E_{in}$  is transferred to  $E_{out}$ )  $E_{out29} < E_{in30}$ ; therefore, voltage at node 36 is greater than at node 39; consequently transistor 21 is held in a conducting state, while voltage at node 35 is greater than the voltage at node 39; consequently transistor 23 is held off. It will be shown that  $\beta i_{g41} \cong i_{o27}$ .

The above process continues until the output voltage  $E_{out29}$  approximately equals the input voltage  $E_{in}$ , that is, the legs of the bridge assume a balanced condition. When  $Z_{o32}$  is a capacitor, it charges to the input voltage by means of current  $i_{g41}$ . If  $E_{out29}$  exceeds  $E_{in30}$ , transistors 22 and 23 are biased to conduct and transistors 21 and 24 are cut off to restore a balanced condition.

$E_{in} \cong E_{out}$  when the current generators 25 and 26 are switched on, indicating a unity voltage gain. The output circuit is completely isolated from the input circuit when  $i_{g41}$  and 42 are not flowing; as a result,  $i_{g41}$  and 42 act as a control gate on the signal transfer from input to output.

During signal transference, transistors 22 and 23 are cut off. As a consequence, the following relationships apply:

At node 38;  $i_{g28} = i_{b8}$  for  $i_{b9} = 0$

At transistor 24:  $i_{b8}$  flows into the base, and  $\beta i_{b8}$  flows into the collector; therefore  $(\beta + 1)i_{b8}$  flows out of the emitter.

At node 35 then;  $(\beta + 1)i_{b8} = i_{g42}$  for  $i_{b7} = 0$

Substituting  $i_{s28}$  for  $i_{b8}$ ;  $(\beta + 1)i_{s28} = i_{g42}$

Also at node 36;  $i_{g41} = i_{b6}$  for  $i_{b9} = 0$

At transistor 21:  $i_{b6}$  flows into the base, and  $\beta i_{b6}$  flows into the collector; therefore  $(\beta + 1)i_{b6}$  flows out of the emitter.

At node 39:  $(\beta + 1)i_{b6} = i_{o27}$  for  $i_{b7} = 0$

Substituting  $i_{g41}$  for 6;  $(\beta + 1)i_{g41} = i_{o27}$ , and

$$i_{g41} = \frac{i_{o27}}{\beta + 1}$$

$i_{g41} = i_{g42}$ , therefore:

$$(\beta + 1)i_{s28} = \frac{i_{o27}}{\beta + 1}$$

and  $i_{o27} = (\beta + 1)i_{s28}$ , or if  $\beta$  is much greater than one  $i_{o27} = \beta^2 i_{s28}$ , current gain for the overall circuit is  $\beta^2$ .

Three fundamental differences between the present invention and the conventional bridge are now apparent. These differences are the use of active elements in the bridge, the symmetrical current sources 25 and 26, and the overall current gain of the circuit.

It will be further noted that if the polarity of  $E_{in30}$  is reversed, transistors 22 and 23 will be switched on while 21 and 24 are held off, but the overall operation remains the same. Furthermore, transistors 22 and 23 are shown as PNP type transistors while transistors 24 and 21 are shown as NPN. The circuit could be reversed, making transistors 24 and 21 PNP types and transistors 22 and 23 NPN types without detracting from the effective operation of the circuit.

Two current generators 25 and 26 are shown. Their midpoint is grounded resulting in symmetrical currents. Alternatively, a single ungrounded current source between nodes 36 and 35 may be utilized. In any event, the current source contemplated must have at least a plus or minus one percent regulation; that is, a relatively constant current source is needed.

Referring to FIGURE 2, a slight modification of the circuit shown in FIGURE 1 is illustrated. This circuit offsets the output voltage with respect to the input so as to provide a predetermined difference between output and input voltage.

Rectifier 53 in the leg containing transistor 21 together with rectifier 54 in the leg containing transistor 24 raises the voltage of the output V52 such that

$$V_{in51} + V_{offset} = V_{out52}$$

where  $V_{offset}$  is the desired voltage offset introduced by means of rectifiers 53 and 54.

The above is one method by which an offset can be introduced. A voltage offset may also be provided by applying a fixed potential at the output terminal 55 such that the output voltage 52 is the sum of the voltage produced by the transistor bridge network and the fixed potential. Obviously, the output voltage can be raised or lowered with respect to the input. In other words, negative as well as positive offset can be introduced.

Referring to FIGURE 3, it will be observed that an impedance has been inserted in the collector circuit. With a voltage threshold applied to the output terminal 59, transistor 21 will remain off until  $V_{in58}$  exceeds this voltage. When  $V_{in58}$  becomes greater than V59, current flows in the collector circuit of transistor 21 and a voltage  $V_{out61}$  develops across impedance Z62. It will be further noted that a negative threshold will be established by the insertion of an impedance in the collector circuit of transistor 23 and an appropriate threshold voltage applied at 59.

The foregoing has been directed to networks wherein the four legs of a network are transistors. While the use of transistors or other solid-state amplifiers in each leg is preferred, certain substitutions can be made in the legs. If the two opposing transistors are replaced with diodes, input signals will be power amplified in only one direction either positively or negatively depending upon which group of transistors is replaced. If adjacent transistors are replaced by two diodes then the amplification factor of the bridge will be reduced to  $\beta$ . If other passive elements are used in place of diodes, isolation is sacrificed.

FIGURES 1, 2 and 3 represent three basic building blocks: a straight through network illustrated in FIGURE 1, an offset voltage circuit illustrated in FIGURE 2, and a threshold circuit in FIGURE 3.

These various circuit configurations or building blocks may be usefully employed in numerous applications and devices. For ease in describing and illustrating such applications, the various configurations will first be identified symbolically, according to FIGURES 4A-E.

FIGURE 4A shows a straight-through bridge. Current input appearing at terminals 63 and 64 control the

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circuit and gate it "on" or "off." This current can be gated or continuous. When in the "on" mode, an input signal applied to terminals 60 will effectively transfer to terminal 65, the output terminal. The signal at this point experiences power gain without a change in signal level. It is to be noted that the current terminals have open centers and can therefore be readily distinguished from the voltage terminals which have solid centers throughout all the illustrations.

FIGURE 4B shows a similar circuit; however this circuit introduces a positive offset in the output voltage. That is, the output will now be some prescribed voltage higher than the applied voltage. FIG. 4C shows a circuit with negative offset. Positive and negative offset are indicated by arrows 12 and 13 respectively.

FIGURE 4D again shows a circuit similar to those preceding. Here, an input voltage applied to terminal 87 is effectively compared with a threshold voltage that may be applied to terminal 88. When the input voltage reaches the level of the threshold voltage a pulse is generated in the collector circuit of the transistor connected between terminals 63 and 88 as indicated by arrow 14. FIGURE 4E shows a circuit generating a pulse as indicated by arrow 15 when a negative voltage is applied to terminal 89.

Using the above symbolic representations, several representative applications will now be described in conjunction with FIGURES 5A-J.

In FIGURE 5A, a voltage amplifier is shown.  $V_{in71}$  is applied to the bridge circuit and impedance  $Z_172$  in series.  $V_{out74}$  is taken across both impedance  $Z_172$  and  $Z_273$ . A constant current is applied to the bridge at terminals 63 and 64 unless it is desired to have the output gated. The voltage amplification for this circuit is:

$$A_v = \frac{1}{\frac{1-Z_2}{Z_1+Z_2}}$$

The above unit may be used as an A.-C. amplifier or a D.-C. amplifier. In either case feedback is present and a voltage gain greater than unity is obtained. Several other function generators may be provided by this configuration. Using feedback techniques, voltage functions with respect to time can be generated. Further, using variable-offset circuits in which the offset is controlled by feedback from the output level, a variety of useful functions can be generated. For instance, a linear slope generator, a delay circuit, and even a ladder circuit generator can be constructed.

FIGURE 5B shows a threshold detection circuit which functions like a Schmitt trigger. For example, if a constant voltage  $V_{in75}$  is applied to the circuit and a fixed voltage  $V79$  applied to the bridge at its usual output terminals, current pulses 76 and 77 applied to the circuit will cause an output 78 to appear only when  $V_{in75} > V79$ . A very flexible trigger is now available in that the threshold voltage  $V79$  can be readily changed without disturbing the rest of the circuit, a feature not found in conventional Schmitt triggers.

In FIGURE 5C a storage system is shown. A voltage input  $V_{in80}$  will be transferred any number of units down, provided gates  $P_{in81}$  and 83 are switched on. When  $P_{in81}$  is switched on,  $V_{in80}$  transfers to  $C_182$  and held. When  $P_283$  is switched on,  $V_{in80}$ , now at  $C_182$ , transfers to  $C_284$ . When the stored information is desired,  $P_n$  and any preceding units must be gated on. Accordingly, when  $P_n85$  is switched on, voltage  $V_{in80}$  now at  $C_284$  will be transferred to  $C_{out86}$ .

FIGURE 5D shows an analog addition system. Assume a signal voltage  $V_192$  is to be added to  $V_293$ . Signal  $V_192$  is applied to bridge 94. When bridge 94 and bridge 98 are switched on simultaneously by means of gate pulse  $P_1100$ ,  $V_192$  is transferred to  $C_196$  and held there. When bridge 95 is switched on by means of pulse  $P_2110$ ,  $V_293$  is transferred to  $C_297$ . Read out

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$V_099$  will be across  $C_297$  and  $C_196$  and will indicate the sum of the two voltages  $V_192$  and  $V_293$ .

FIGURE 5E shows analog subtraction.  $V_2101$  is transferred to  $C_2106$  by way of 103.  $V_1102$  is transferred to  $C_1$  by way of 104. Ground in both instances is transferred to the midpoint of  $C_2106$  and  $C_1105$  by way of 108. 103, 104 and 108 would be switched on simultaneously by means of a current pulse applied to them individually from a common current source. 107 is then switched on for read-out.  $V_2$  is read across  $C_2$  in the forward direction and  $V_1$  is read across  $C_1$  in the negative direction; consequently, 109 indicates the difference in the two signals.

FIGURE 5F shows digital addition. Assume, for the moment that no voltage appears across  $C114$  or  $C113$ . When a pulse  $P_1111$  appears at bridge 116,  $C113$  increases its voltage as a result of the offset, indicated by the arrow. If the indicated offset is 1 volt,  $C113$  receives a 1 volt charge. The voltage across  $C113$  is thereupon transferred to  $C114$  by way of bridge 115 which is continuously switched on at prescribed intervals.

If the above pulse  $P_1111$  is, by way of example, a train of five pulses, for each of these pulses the capacitor  $C113$  receives a charge one volt greater than  $C114$  due to the offset. Bridge 115 then transfers the increased voltage to  $C114$ , raising it to the same voltage as  $C113$ . When the next pulse in the train arrives,  $C113$  again is charged one volt higher than  $C114$ , but  $C114$  is now at a higher voltage than it was due to the previous pulse. Ultimately, both capacitors become charged to 5 volts.

Likewise, if  $P_2112$  is a train of three pulses, the offset of 117, which is identical to that of 116, causes capacitors 113 and 114 to become charged an additional 3 volts. The sum of pulse trains 111 and 112, eight volts, is at 118 for read-out.

FIGURE 5G shows digital subtraction, with bridge 128 providing a negative offset. That is, when a pulse is applied to 128 from  $P_2121$ , the voltage across  $C125$  is reduced. Accordingly, bridge 124 will cause capacitors 125 and 122 to charge to 5 volts if the offset is again one volt and  $P_1120$  is a train of five pulses. If  $P_2121$  is a train of three pulses, bridge 128 will reduce the voltage across  $C125$  and  $C122$  by three volts. Therefore read-out 126 will be the difference of these two voltages or two volts in this instance.

FIGURE 5H shows digital-to-analog conversion. Register 131 causes multivibrator 132 to pulse bridge 133 a prescribed number of times. Again, bridge 133 has an offset. For convenience assume one volt. If the voltage across  $C_s135$  and  $C_L136$  is zero, bridge 133 will cause  $C_L$  to increase its voltage by one volt greater than  $C_s135$ . However, as  $C_L136$  charges up one volt higher, by means of resistor 134,  $C_s135$  also charges up to the increased voltage a short while later. The increase continues with each pulse producing an analog output  $V_{out137}$  which will appear as waveform 138.

FIGURE 5J shows analog-to-digital conversion. Analog input  $V141$  is applied to bridge 142 and is transferred to  $C_s150$ .  $C_L148$  charges up to the same voltage as  $C_s$  by way of resistor 149. Multivibrator 143 switches on 144 and 145 alternately. When 144 is switched on, the voltage across  $C_L148$  is reduced one volt. A path to ground for the discharge of the difference in voltage is provided by means of bridge 145. The process continues until the voltage across both capacitors  $C_s150$  and  $C_L148$  is reduced to zero. The number of times "n" that this will occur is:

$$n = \frac{V_{in141}}{\Delta V}$$

where  $\Delta V$  is the voltage offset of bridge 144. Each time that 145 is switched on and a voltage difference on  $C_L148$  passed to ground 147 a positive pulse is generated across the impedance threshold inserted in the collector of 145

as explained earlier and consequently registered at register 146.

The performance of a given transistor network is very much affected by its components. This can be seen by an examination of three formulae:

(1) For speed,  $S_p = \frac{P_{ave}}{S}$  (bits second)

(2) For power requirements,  $P_{ave} = K S \frac{4V_c^2}{R_o}$

(3) For stability,  $S = \frac{1}{(V_s/V_o) + (V_d/V_o) + (V_t/V_o)}$

where;  $S_p$  = speed;  $P_{ave}$  = average power;  $S$  = stability;  $K$  is a constant;  $V_c$  the gate supply voltage;  $R_o$  the output impedance of the bridge;  $V_s$  the change in input voltage due to sampling;  $V_o$ , the minimum change in output voltage due to sampling,  $V_d$  the voltage transfer uncertainty due to variation in emitter base structure;  $V_t$ , change in output due to discharge in  $C_o$ , an output capacitor through  $R_o$  during time interval  $T$ .

The transistor bridge is extremely fast and requires little power. However, if an unusual requirement in one or the other is made, an inspection of the first two formulas indicates one must be sacrificed for the other. Stability is also reflected in the determination of speed and power needs. Stability determines the accuracy of the device and hence is of prime importance. Speed and power requirements can usually be neglected and a very satisfactory device will nevertheless be produced, while concentrating entirely on stability.

From the third formula, stability is determined by three factors. The first is input stability and is indicated by the ratio  $V_s/V_o$ . This ratio is kept to a minimum by matching the impedance placed across the input terminals with that of an impedance placed across the output terminals. In practice, this factor is of little significance.

The second factor affecting overall stability is offset stability and is indicated by the ratio  $V_d/V_o$ . With a proper selection of matched transistors, this ratio can be kept to a minimum. In practice, with little effort one millivolt has been achieved. It will be noted that this is the most significant factor of the three. However, it may have a positive or negative value and when one or more bridges are tied together is self canceling.

The last factor to be considered is storage stability and is indicated by the ratio of  $V_t/V_o$ . This latter factor is the result of leakage from the output capacitor and is a function of  $C_o$ ,  $R_o$  and time  $T$ . This factor can be kept small by increasing  $R_o$  which is easily done by selecting silicon transistors. Furthermore, it can also be reduced by a proper design in holding time and an appropriate selection of the size of capacitor  $C_o$ . Again this latter factor is relatively small and can be optimized in design.

Many digital systems have been illustrated utilizing the present invention. Such illustrations are merely representative of the diverse uses of my invention in a variety of systems.

I claim as my invention:

1. A bridge network comprising, input means, output means, four transistors,

two of which are NPN transistors, and two of which are PNP transistors, a first group of said transistors comprising an NPN transistor and a PNP transistor having their bases connected together, a second group of said transistors comprising an NPN transistor and a PNP transistor having their emitters connected together,

said first group of interconnected transistors having their emitters connected to the bases of said second group of interconnected transistors, positive and negative biasing means, said PNP transistors having said negative bias applied to its collectors, said NPN transistors having said positive bias applied to its collectors, current generating means for gating said transistors on and off having first and second leads, said first lead of said current generating means connected to one point of connection between said first and second group of transistors, said second lead of said current generating means connected to the second point of connection between the first and second group of transistors, said input means connected to said base connections of said first group of transistors, said output means connected to said emitter connection of said second group of transistors.

2. A transistor bridge according to claim 1 wherein said current generating means is two symmetrical current sources connected in series with the midpoint connection between said symmetrical current sources grounded,

said symmetrical current sources being so arranged as to be of instantaneous opposite polarity, with respect to ground, said current sources having a regulation of at least plus or minus one percent.

3. A transistor bridge network according to claim 2 which further includes,

an input impedance having first and second leads, said first lead of said input impedance connected to the point of connection between the bases of said first group of interconnected transistors, said second lead of said output impedance connected to ground,

an output impedance having first and second leads, said first lead of said output impedance connected to the point of connection between the emitters of said second group of interconnected transistors, said second lead of said output impedance connected to ground, said input and output impedance being substantially identical.

4. A transistor bridge network according to claim 3 which further includes two rectifiers in the emitter circuit in series with two similar in type transistors whereby the output will be offset a predetermined increment from the input.

5. A transistor bridge network according to claim 4 which further includes an impedance inserted in the collector circuit of a preselected transistor whereby thresholds can be detected.

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